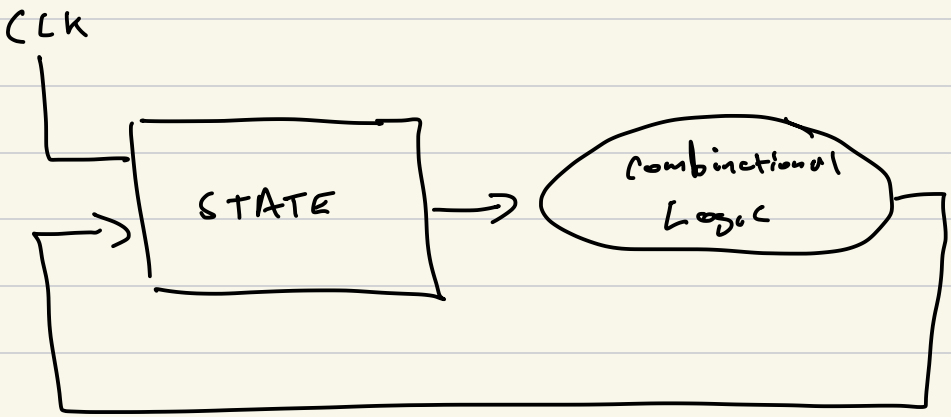
CS 631-01 Processor Design Components

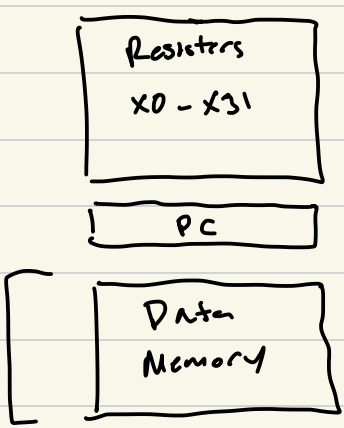
Project04 Q & A

Complete Processor Micro architecture

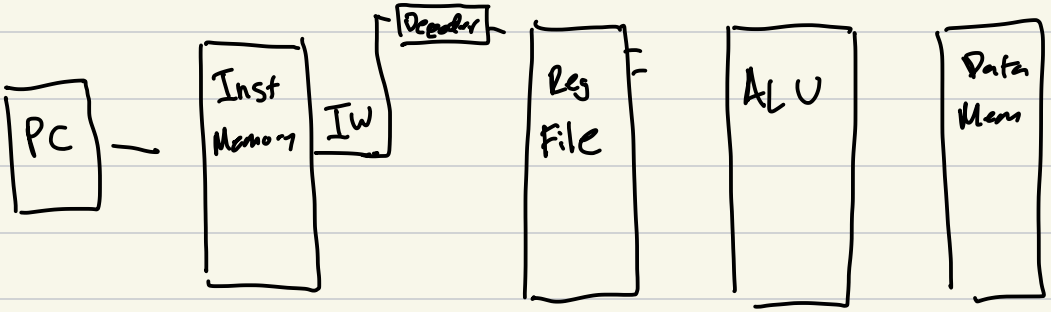


Processor

STATE



Processor Components



Single-cycle processor

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multi-cycle processor

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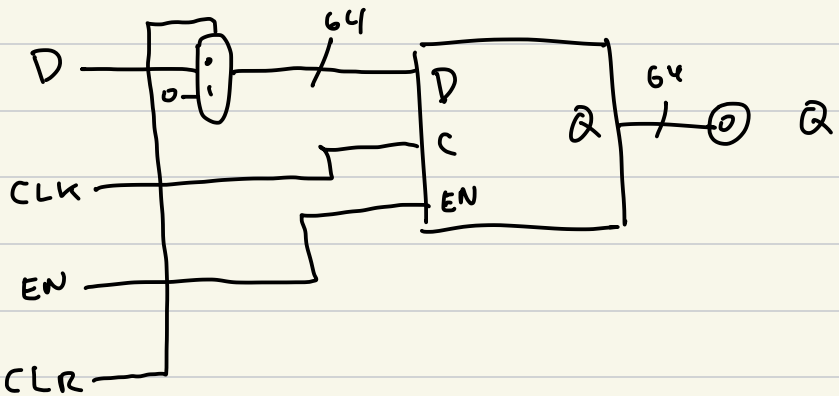
pipelined processor

Moore's Law # of transistors doubles every 1.5 years

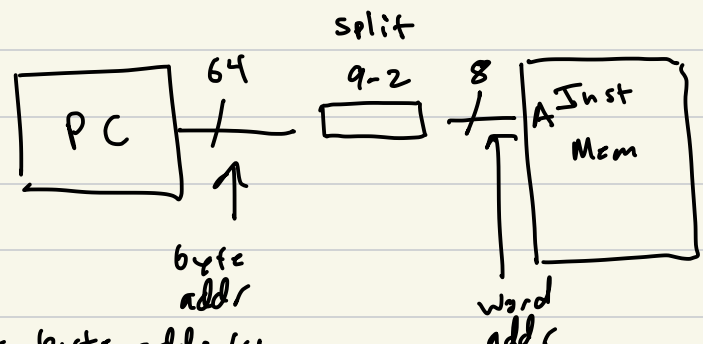
PC Program Counter

64-bit Register

Digital Register with CLR (Synchronous)



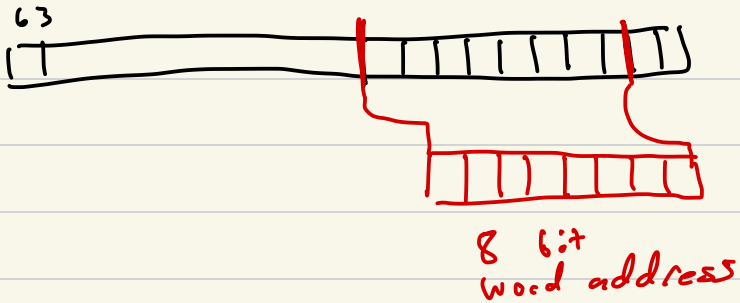
Instruction Memory



word_addr = byte_addr / 4

= byte_addr >> 2

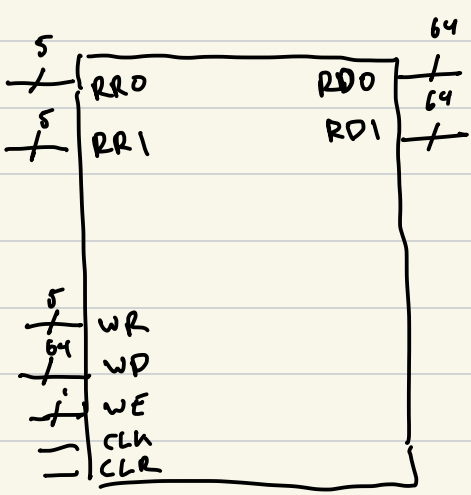
byte addr 64 bits



Register File

32 64-bit Registers: $X0, X1, \ldots, X31$

Read up to two register values on a single clock cycle. Write up to one register on a clock cycle. X0 will always be 0.



RR - read reg #

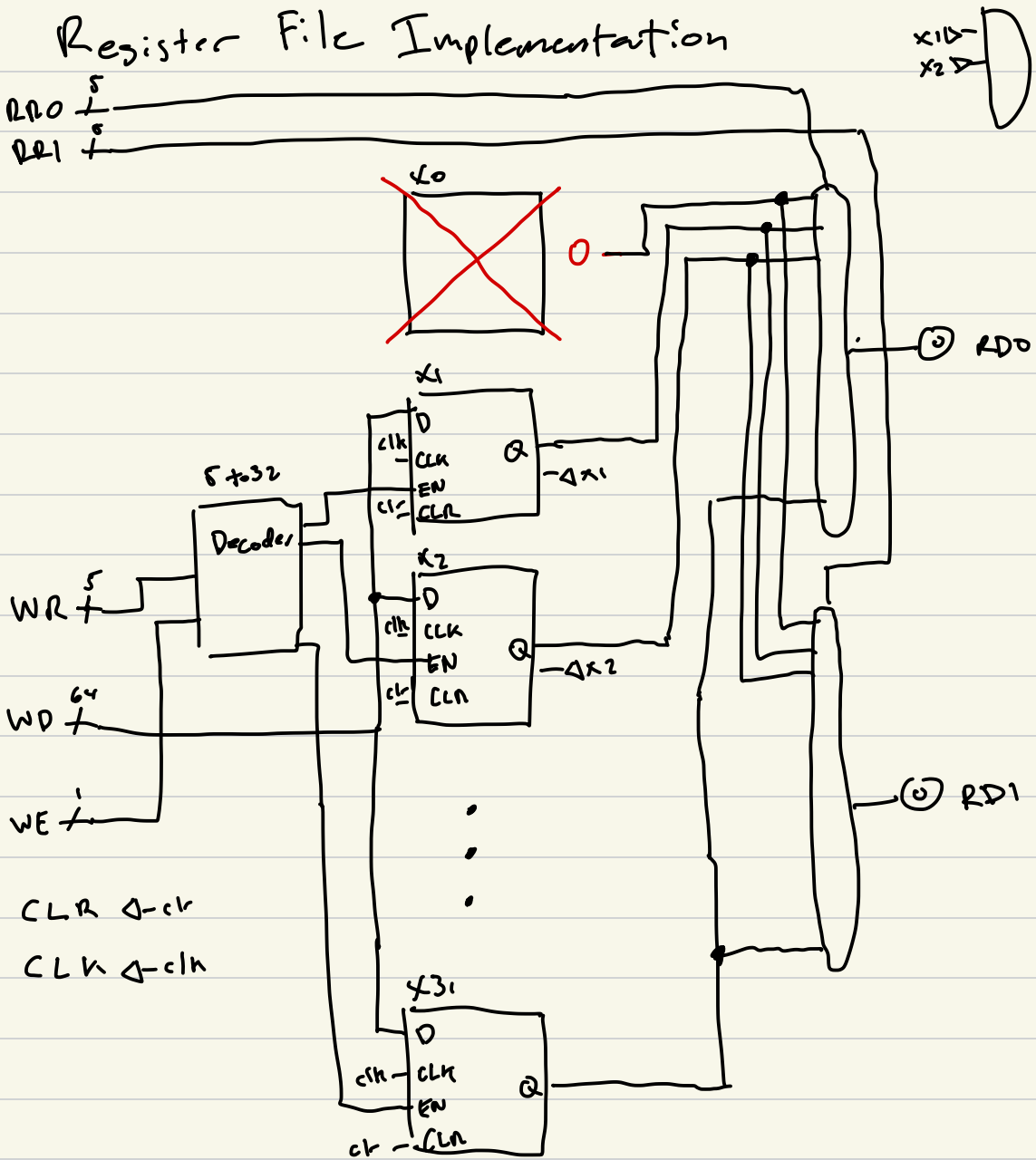
RD - read data

WR - write reg

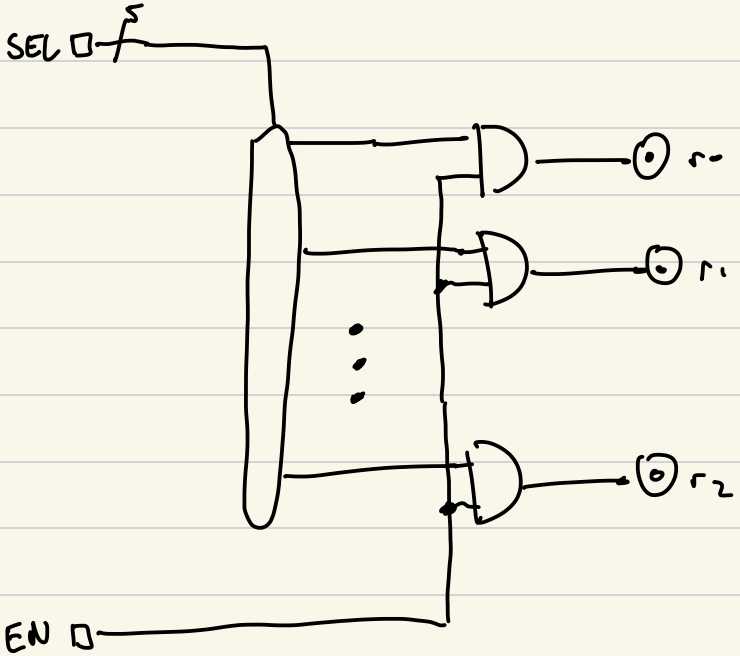
WD - write data

WE = write enable

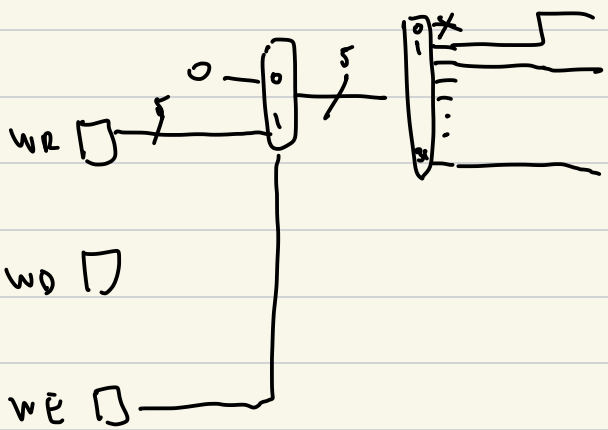
Register File Implementation



Decoder with Enable



MUX approch for EN



ALU Arithmetic Logic Unit